INTRODUCTION

The hiFace Evo is provided with an I²S output which allows for low-jitter, high-quality connection to D/A converters provided with an I²S input.
Alas, aside the signals set, no standard is provided for an extra-equipment I²S connection. Various voltage standards, pinouts and connectors are used in various D/A converters which make the connection with hiFace Evo more difficult.
This application note focuses on signals voltage and format adaptation in order to have hiFace Evo working with all D/A converters on their I²S input. The user is supposed to be acquainted with the various connectors and the most common voltage standard used in this application.

VOLTAGE STANDARDS AND CONNECTORS

Various standards and connectors are used for I²S inputs on D/A converters. Amongst voltage standards:

- TTL/CMOS single-ended
- TTL/CMOS differential
- LVDS
- ECL

LVDS is becoming widely used on commercial D/A converters because of its immunity to noise and capability to drive long cable runs. TTL/CMOS single-ended is more common on DAC boards for DIY'ers. hiFace Evo offers a simple 3.3V CMOS (5V TTL compatible) output. Amongst connectors:

- RJ-45
- HDMI
- Strip

The HDMI connector is generally associated with LVDS format (but this is not necessarily true, so please check specifications before assuming that LVDS levels are carried in on an HDMI connectors), while RJ-45 and the strips are more commonly used with single-ended and differential formats. hiFace Evo uses an RJ-45, 8 pins connector with the following pinout (left to right):

1) SDATA
2) GND
3) LRCK (FS)
4) GND
5) SCLK (BIT CLOCK)
6) GND
7) MCLK
8) GND

Signals are LVCMOS, that is CMOS levels at 3.3V supply. They are TTL-compatible, that is, they can directly drive a 5V TTL input stage without need for level translation. The hiFace Evo's I²S output is drive by a high current driver, so it can directly feed an input when no level translation is needed.

MCLK USAGE

The hiFace Evo's Master Clock (MCLK) is made available on the Evo's I²S output. It may be necessary on some D/A converters, particularly when no local Master Clock is available. Depending on the sampling frequency, the Evo outputs two different Master Clock frequencies: 22.5792MHz for files with 44.1, 88.2 and 176.4kHz sampling frequency and 24.576MHz for files with 48, 96 and 192kHz sampling frequency. Thus, the MCLK/LRCK ratio depends on the sampling frequency: it is 512x with 44.1 and 48kHz files, 256x with 88.2 and 96kHz files and 128x with 176.4 and 192kHz files. Should your D/A converter use the Evo's Master Clock and need a fixed ratio (for example, 256x or 128x) at all frequencies, a selectable frequency divider or multiplier should be used.
A frequency divider (Fig. 1) is easily made using D-type flip-flops like TI's SN74LVC74 (double flip-flop which allows for 2 times and 4 times clock frequency division), while a PLL (Fig. 2) must be used to double the Master Clock, such as Cypress' CY2300 (BTW, the CY2300 is perfect to have a fixed 256x ratio, as it offers both 2x and 1/2x frequency outputs, along with buffered 1x output).

3.3V TO 5V LEVEL TRANSLATION

When a 5V CMOS input circuit is to be driven, a simple level translation can be done by using a quad non inverting buffer with TTL

input compatibility, such as the SN74HCT125 by Texas Instruments (Fig. 3).

SINGLE-ENDED TO DIFFERENTIAL CONVERSION (TTL OR CMOS)

Some D/A converters accept differential signals on their I2S input (such as NorthStar Design units). In this case, no simple level translation (even if a level translation can be necessary, too) can accommodate the D/A converter's input requirement. A format conversion is necessary. It can be performed using a inverting/non inverting buffer pair in order to achieve an inverted copy of each signal to drive a line in a balanced fashion (Fig. 4). The non-inverting buffer is necessary to introduce a small delay on the original signal to match (not perfectly, but to a satisfactory extent) that introduced by the inverting buffer. For non-inverting buffers, go for the usual SN74HCT125 (for 3.3V to 5V translation) or the SN74LVC125 (no level translation). Inversion and buffering can be obtained by simply using four units of an hex inverter such as TI's SN74HCT04 (level translation) or SN74LVC04 (no level translation).

SINGLE-ENDED to LVDS (HDMI) CONVERSION

Some D/A converters (such as PS Audio PWD) accept LVDS signals on an HDMI connector. To perform a single-ended to LVDS conversion, National's DS90C031B can be used (Fig. 5). It is a quad LVDS driver with TTL input compatibility which can be directly coupled to hiFace Evo's output.

TYPICAL APPLICATION CIRCUITS

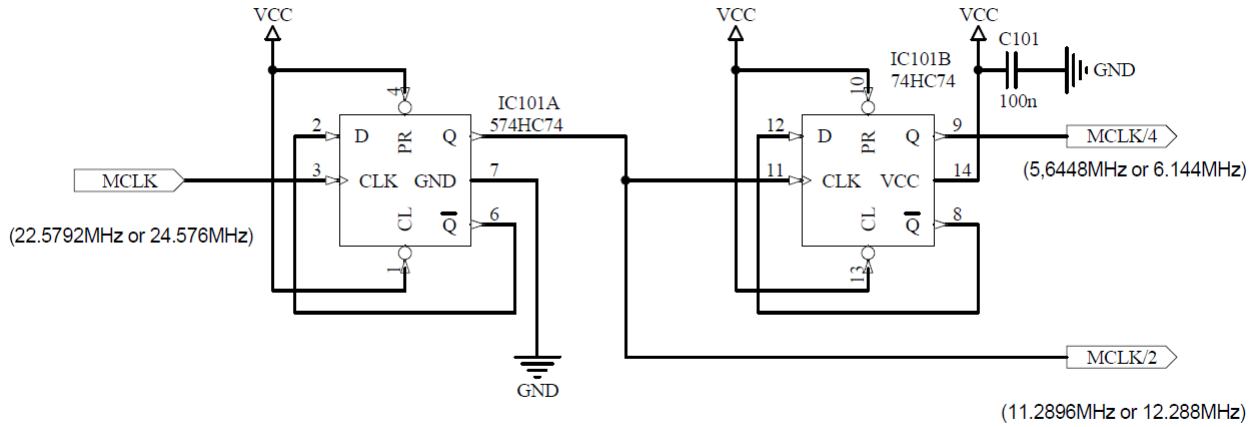

Figure 1. Master Clock Divider

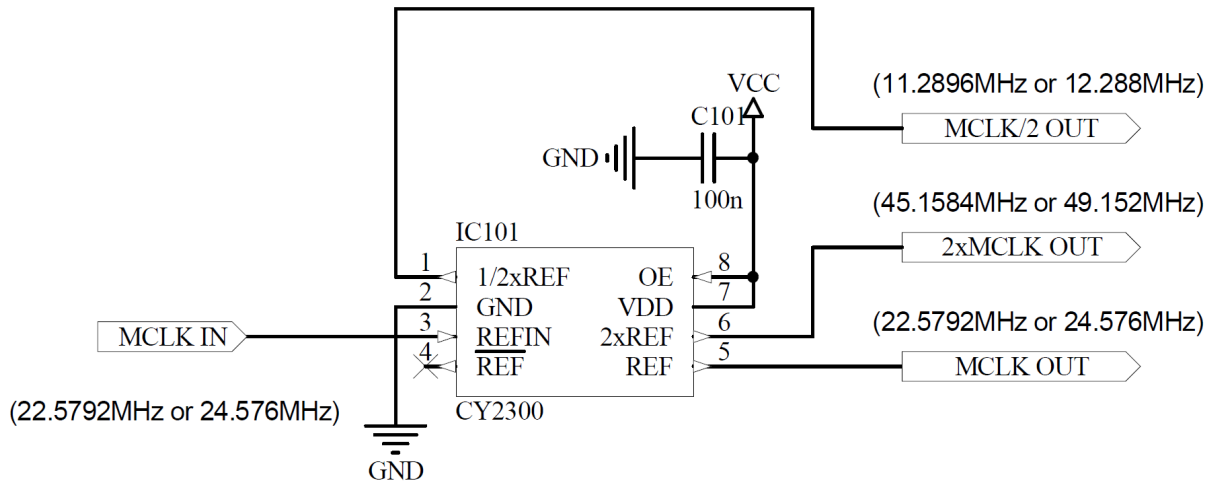

Figure 2. Master Clock multiplier with CY2300

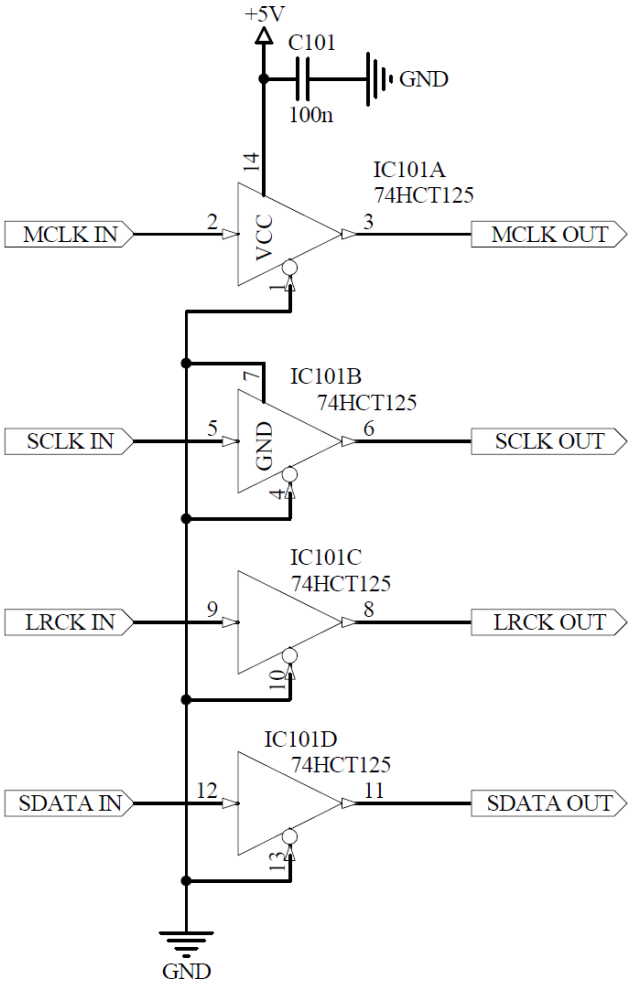

Figure 3. 3.3V to 5V level translation

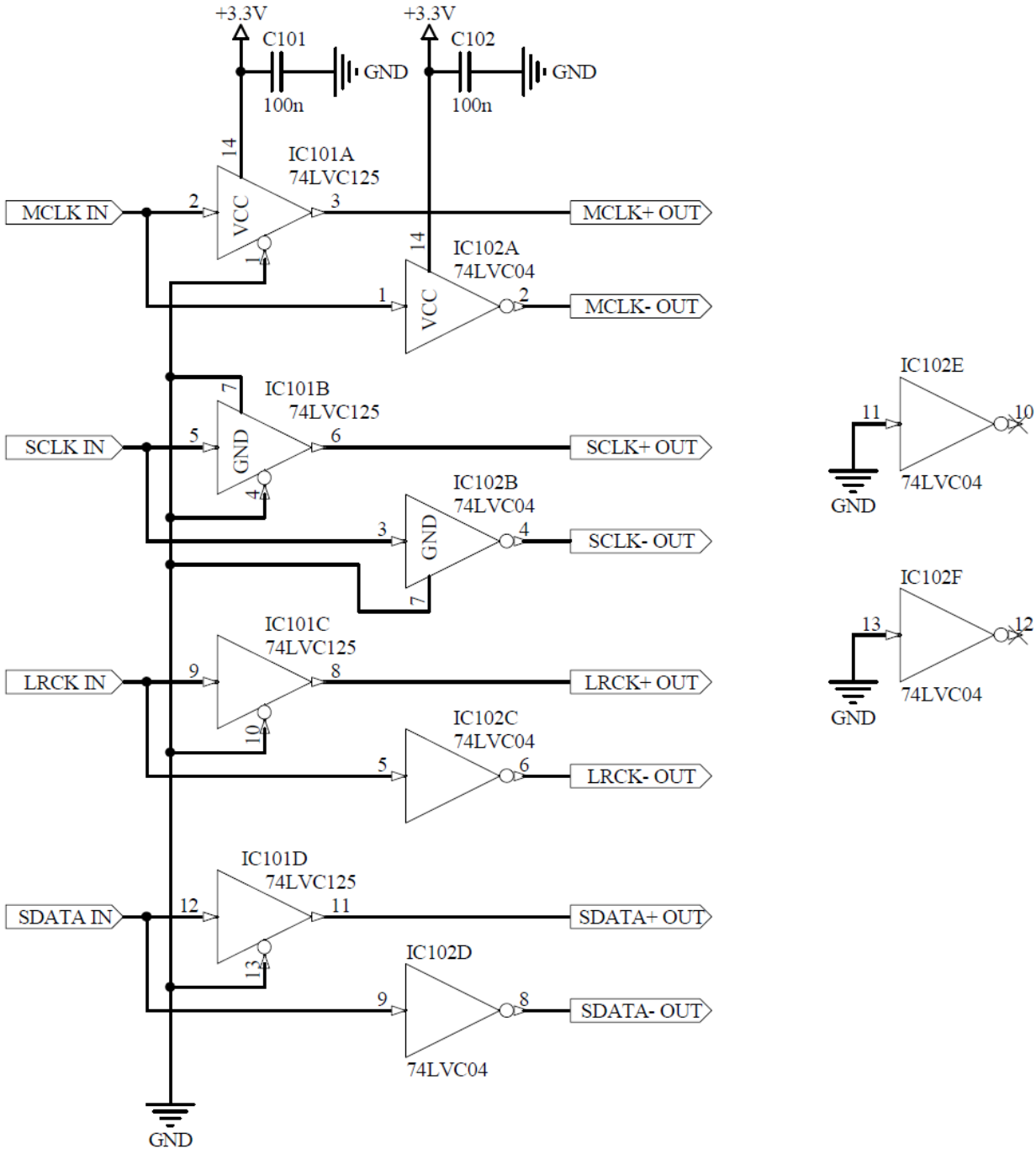

Figure 4. Single-ended to differential conversion

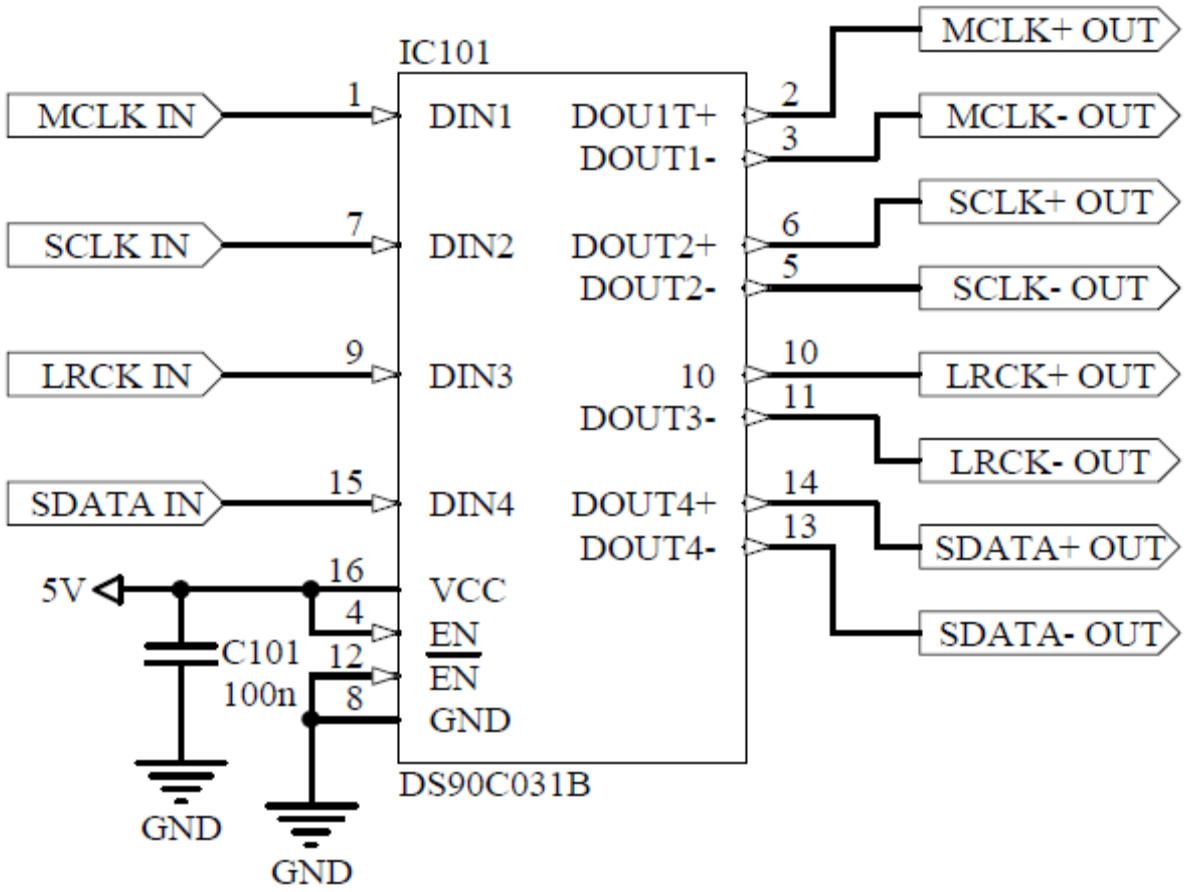

Figure 5. Single-ended to LVDS conversion

REFERENCES

hiFace Evo User Manual (http://www.m2tech.biz/public/pdf/hiFace%20Evo%20user%20manual%201-0.pdf)
Cypress CY2300 (http://www.cypress.com/?rID=13287)
Texas Instruments website for various IC's (www.ti.com)
National DS90C031B (http://www.national.com/mpf/DS/DS90C031B.html#Overview)

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