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M2TOEM-02
MASTER CLOCK & WORD CLOCK PROGRAMMABLE GENERATOR

REVISION PrB - JUNE 2012

FEATURES

- **Up to 384kHz word clock out**
- **Up to 24.576MHz master clock out**
- **64x, 128x and 256x "super clocks"**
- **Low phase noise TXCO's**
- **Hardware and software control**
- **SPI port for software control**
- **Two outputs (master and word) with separate setting**
- **LVCMOS 3.3V outputs**
- **Single supply**
- **Small form factor (45.7 x 28 mm)**

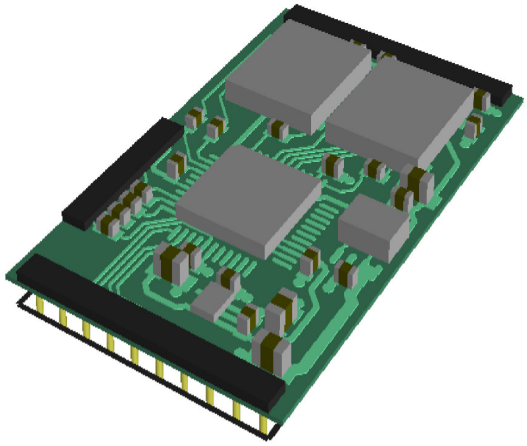
APPLICATIONS

- **High performance audio digital sources**
- **High performance audio DAC's with master clock option**
- **Word clock generators**

DESCRIPTION

M2TOEM-02 is a high performance, low phase noise clock generator for audio use.
It features two low phase noise, high stability TCXO's as time base and a flexible divider with two outputs.
Both hardware and software control is possible. Hardware control is accomplished by pin strapping, while software control is performed by an SPI interface.

Two female strip PCB connectors carry all clock, supply and control signals for an easy integration on a motherboard.
Two on-board, ultra-low noise regulators produce all the voltages necessary to operation from a single supply.



ORDERING INFORMATION(1)

T_j	PART NUMBER
0-50°C	M2TOEM-02

(1) All versions are RoHS compatible.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply voltage range (with respect to GND)	V_{cc}	12	V
Output current	any output pin	10	mA
V_{IH}	Any input pin	-0.3 3.6	V
T_A Operating free-air temperature range		0°C to 50°C	°C
T_j Junction temperature range		0°C to 70°C	°C
T_{stg} Storage temperature		-40°C to 125°C	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the devices on the board. These are stress ratings only, and functional operation of the devices on the board at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect board reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{cc}	4	5	10	V
Operating junction temperature range, T_j	0		50	°C

DC ELECTRICAL CHARACTERISTICS

T_j = 0°C to 50°C and recommended supply voltage range (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Outputs unloaded, V_{cc} = 5V		10	60	mA
V_{OH}	MCLK, WCLK pins, I_{OH} = -8mA	2.9			V
V_{OL}	MCLK, WCLK pins, I_{OL} = 8mA			0.4	V
V_{IH}	All input pins	2.0			V
V_{IL}	All input pins			0.8	V

AC ELECTRICAL CHARACTERISTICS

T_j = 0°C to 50°C and recommended supply voltage range (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CCLK				66	MHz
t_{CSCR}		5			ns
t_{CDS}		7.5			ns
t_{CDH}		7.5			ns
t_{CFCS}		5			ns
MCLK		2.8224		24.576	MHz
WCLK		0.0441		24.576	MHz
MCLK duty cycle		45		55	%
WCLK duty cycle		45		55	%
Temperature stability				+/-1	ppm
Stability Vs. Vcc				+/-0.3	ppm
Phase noise	10Hz	-100			dBc/Hz
	100Hz	-130			dBc/Hz
	1kHz	-145			dBc/Hz
	10kHz	-152			dBc/Hz

J1 PIN DESCRIPTION(1)(2)

PIN	TYPE	NAME	FUNCTION
1, 2	Power	VCC	Supply Input for supply and signals
3, 4, 7, 10	Power	GND	Ground return
5	Input	MOSI/CLKEN	SPI data or clock outputs enable in hardware mode
6	Input	CCLK/MCLKSEL1	SPI clock or MCLK select in hardware mode
8	Input	nCS/MCLKSEL0	SPI chip select (active low) or MCLK select in hardware mode
9	Input	H/S	Control mode select

J2 PIN DESCRIPTION(1)(2)(3)

PIN	TYPE	NAME	FUNCTION
1, 3, 5, 10	Power	GND	Ground return for signals
2	Output	WCLK	Word clock output
4	Output	MCLK	Master clock output
6	Input	CLKMUX	Base frequency select in hardware mode
7	Input	WCLKSEL0	WCLK select in hardware mode
8	Input	WCLKSEL1	
9	Input	WCLKSEL2	

(1) The third connector is for factory test only and is not used during normal operation
(2) Pin 1 is the square pad.
(3) J2 is the connector closer to the TCXO's.

TYPICAL APPLICATION CIRCUITS

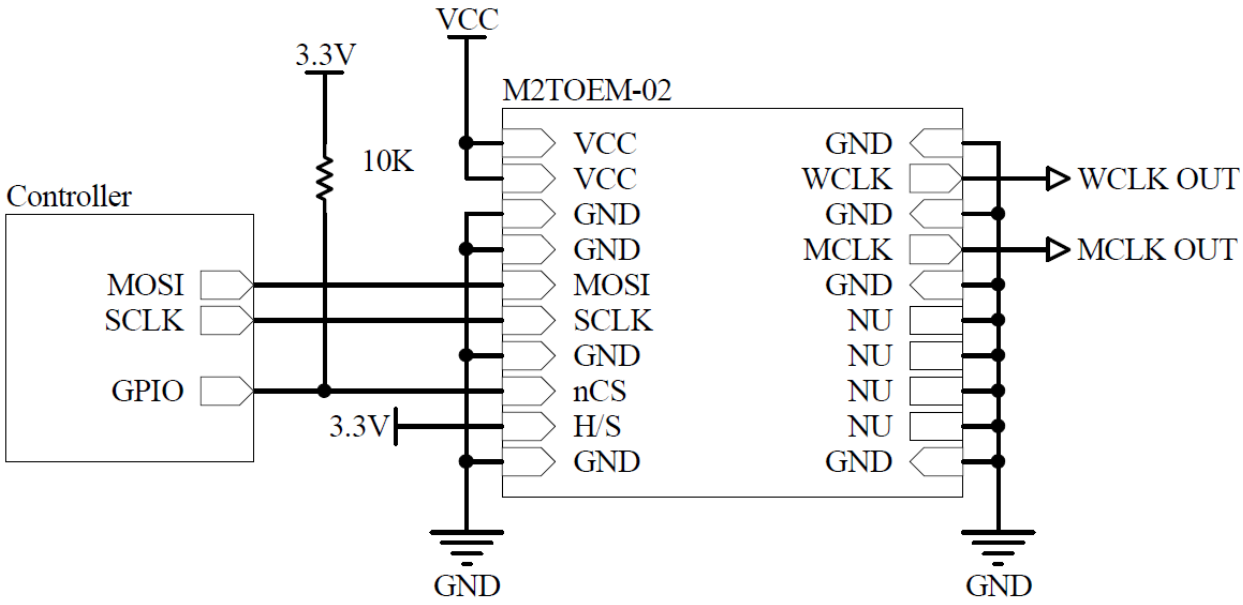


Figure 1. Software control mode

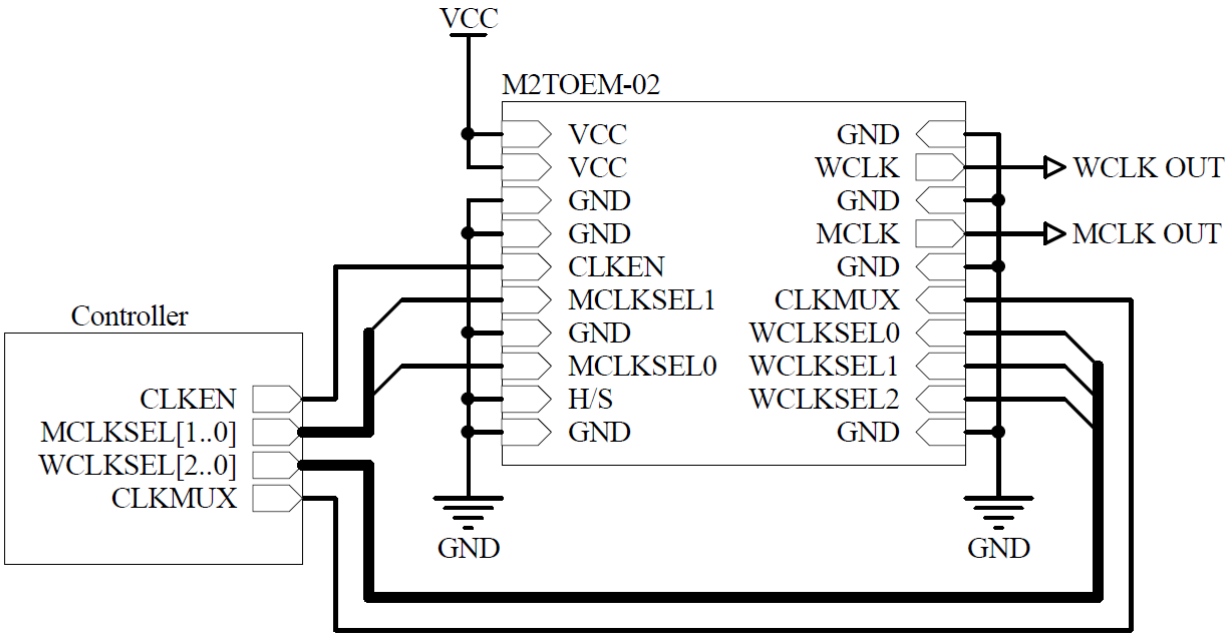


Figure 2. Hardware control mode

THEORY OF OPERATION

The M2TOEM-02 is basically a double TCXO oscillator with very high precision and very low phase noise even at low displacement frequencies (thus a very low jitter), plus a programmable divider. All sensible parts are powered via ultra-low noise regulators, to avoid injecting jitter through the supplies. In fact, even the best oscillator is unable to reach its potential performance if a poor supply with ripple and noise is used to power it.

The two outputs of the M2TOEM-02 are synchronous, meaning that their clocks derive from the same oscillator, depending on CLKMUX setting. This is very useful to provide a circuit with both a master and a word clock. For example, typical CD transport circuits generally need a master clock in the range 11.2896MHz to 22.5792MHz and a 44.1kHz word clock. It is not possible to derive the master clock from one oscillator and the word clock from the other one using the M2TOEM-02.

The M2TOEM-02 can be used in hardware mode (settings are applied by pin strapping) or software mode via an SPI interface. The latter allows for a slightly higher versatility in that it allows for separate enable of each output. This way, unused output can be muted to avoid crosstalk and maximize jitter performance.

Both inputs and outputs are LVCMOS compatible. This means that outputs can be coupled to both 3.3V CMOS inputs and 5V HCT inputs. Inputs need to be driven with 3.3V CMOS drivers.

In order to minimize ringing and related jitter, it is advisable to keep capacitive loads as low as possible, buffering clocks outputs right downstream the pins before distributing them to the circuit. Avoid male-female strips coupling and sold male strips directly to the board and the PCB to reduce parasitic inductance.

APPLICATION INFORMATION

The M2TOEM-02 can be controlled in hardware or in software, depending on the setting of pin H/S, as explained in Table 1.

H/S	Control mode
0	Software
1	Hardware

Table 1. Control mode setting

Hardware mode

In hardware mode, the following pins set the various parameters: CLKEN (a.k.a. MOSI), MCLKSEL[1..0] (a.k.a. SCLK:nCS), CLKMUX and WCLKSEL[2..0]. Please refer to Figure 2 for connection details. Unused pins should not be left unconnected. Tie them to GND.

The base frequency, that is the oscillator from which all output frequencies derive, is selected by pin CLKMUX, as indicated in Table 2. 22.5792MHz can be used to produce clocks for the following sampling frequencies: 44.1kHz, 88.2kHz, 176.4kHz and 352.8kHz. 24.576MHz can be used to produce clocks for the following sampling frequencies: 48kHz, 96kHz, 192kHz and 384kHz.

CLKMUX	Base frequency
0	24.576MHz
1	22.5792MHz

Table 2. Base frequency select

The actual MCLK frequency output on MCLK pin depends on MCLKSEL[1..0] as reported by table 3. If your system needs a master clock of 11.2896MHz or 12.288MHz, for example, set MCLKSEL[1.0] to “01”.

MCLKSEL[1..0]	MCLK
00	Base frequency
01	(Base frequency)/2
10	(Base frequency)/4
11	(Base frequency)/8

Table 3. MCLK select

The actual WCLK frequency output on WCLK pin depends on WCLKSEL[2..0] as reported by table 4 on next page. When a 44.1kHz WCLK is needed, for example, WCLKSEL[2..0] must be set to “111”. Please note that the WCLK output can also provide a master clock (setting “000”) or a “super clock” 64x, 128x and 256x (settings “001” and “010”) which are same as settings “00”, “01”, “10” and “11” of MCLKSEL[1..0].

WCLKSEL[2..0]	WCLK
000	Base frequency
001	(Base frequency)/2
010	(Base frequency)/4
011	(Base frequency)/8
100	384kHz or 352.8kHz
101	192kHz or 176.4kHz
110	96kHz or 88.2kHz
111	48kHz or 44.1kHz

Table 4. Word clock selection

Both outputs can be enabled or disabled by means of pin CLKEN as reported in table 5. Please note that no separate enable pins are provided. If outputs need to be separately enabled, please select software control mode. Please also note that output are not put in hi-Z when disabled; rather, they are forced low.

CLKEN	Outputs status
0	0
1	Enabled

Table 5. Base frequency select

Software mode

Software mode is chosen by setting H/S low. An SPI interface is enabled, on pins CCLK, MOSI and nCS, to allow shift control bits into the M2TOEM-02 divider. Please refer to Figure 1 for connection details. A single byte must be sent to the board to fully configure it Following is the description of the various fields of the control byte. Reset values are indicated.

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MCLKEN	WCLKEN	CLKMUX	MCLKSEL1	MCLKSEL0	WCLKSEL2	WCLKSEL1	WCLKSEL0
Bit 7							Bit0

bit 7 **MCLKEN**: MCLK output enable
0: MCLK output forced to '0'
1: MCLK output enabled

bit 6 **WCLKEN**: MCLK output enable
0: WCLK output forced to '0'
1: WCLK output enabled

bit 5 **CLKMUX**: base frequency selection
0: 24.576MHz are used as base frequency
1: 22.5792MHz are used as base frequency

bit 4-3 **MCLKSEL**: MCLK frequency select
00: base frequency is output on MCLK pin
01: (base frequency)/2 is output on MCLK pin
10: (base frequency)/4 is output on MCLK pin
11: (base frequency)/8 is output on MCLK pin

bit 2-0 **WCLKSEL**: WCLK frequency select
000: base frequency is output on WCLK pin
001: (base frequency)/2 is output on WCLK pin
010: (base frequency)/4 is output on WCLK pin
011: (base frequency)/8 is output on WCLK pin
100: 352.8kHz or 384kHz is output on WCLK pin(1)
101: 176.4kHz or 192kHz is output on WCLK pin(1)
110: 88.2kHz or 96kHz is output on WCLK pin(1)
111: 44.1kHz or 48kHz is output on WCLK pin(1)

(1) actual frequency depends on bit 5 setting.

SPI interface timing is as follows:

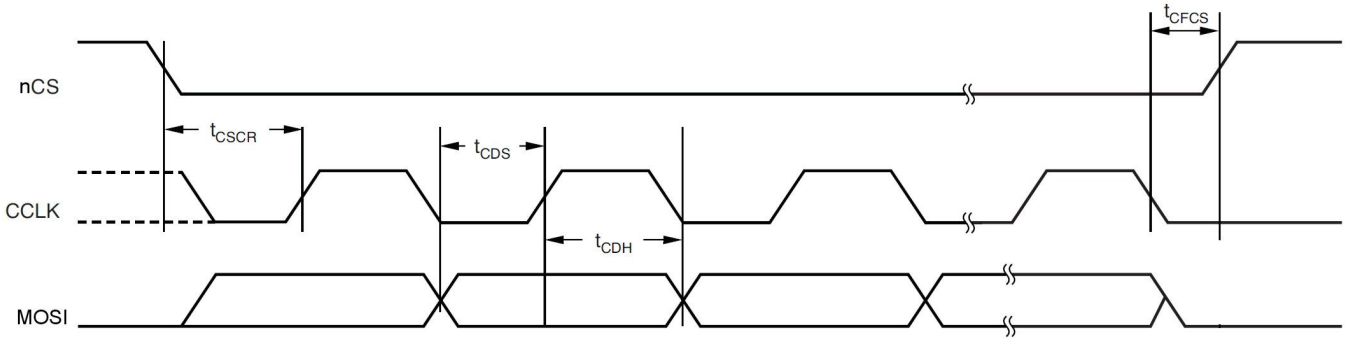


Figure 3. SPI interface timing

MECHANICAL DATA

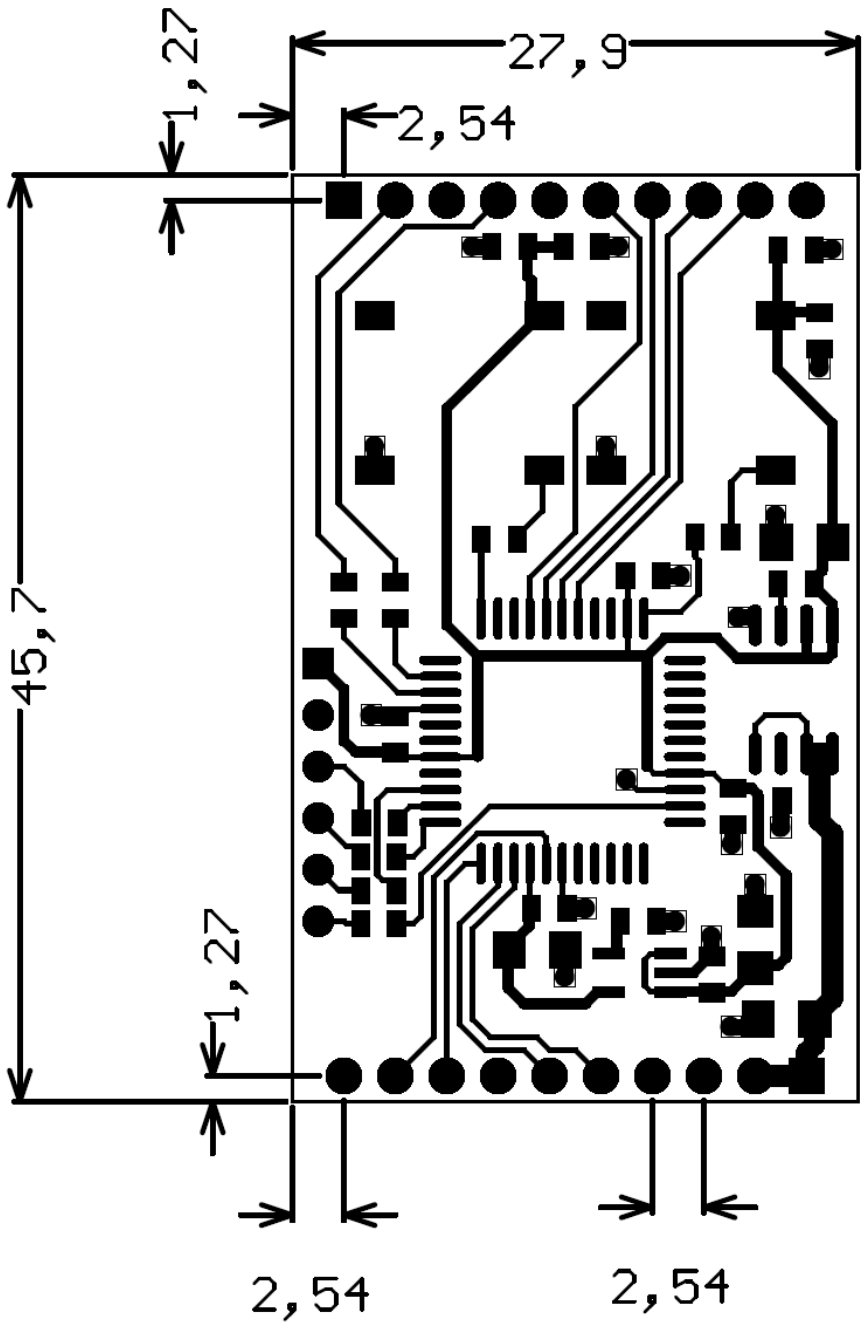


Figure 4. Mechanical drawing. All dimensions are in mm.

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